## Integrated circuit voltage regulators

Objectives: At the end of this lesson you shall be able to

- explain integrated circuit
- state the classification of integrated circuit
- state the types of IC voltage regulators
- design voltage regulator for a required output voltage
- modify fixed voltage regulator to variable output regulator, circuit.


## IC introduction

## Integrated circuit

Electronic circuits invariably consist of a number of discrete components connected to each other in a specific way. For instance, the series regulator circuit discussed in earlier lessons, consists of transistors, zener diodes, resistors and so on, connected in a defined way for it to function as a regulator. If all these components instead of building on a board, if they are built on a single wafer of a semiconductor crystal, then, the physical size of the circuit becomes very small. although small, this will do the same job as that of the circuit wired using discrete components. Such miniaturised electronic circuits produced within and upon a single crystal, usually silicon, are known as Integrated circuits or ICs. Integrated circuits (ICs) can consists of thousands of active components like transistor, diodes and passive components like resistors and capacitors in some specific order such that they function in a defined way, say as voltage regulators or amplifiers or oscillators and so on.

Classification of Integrated circuits: Integrated circuits may be classified in several ways. However the most popular classifications is as follows:

1 Based on its type of circuitry
i Analog ICs-Example: amplifier ICs, voltage regulator ICs etc.
ii Digital ICs - Example: Digital gates, flip-flops, address etc.

2 Based on the number of transistors built into IC
i Small scale integration (SSI) - consists of 1 to 10 transistors.
ii Medium scale integration (MSI) - consists of 10 to 100 transistors.
iii Large scale integration(LSI)-100 to 1000 transistors. iv Very large scale integration (VLSI) - 1000 and above.

3 Based on the type of transistors used
i Bipolar - carries both electron and hole current.
ii Metal oxide semiconductor (MOS) - electron or hole current.
iii Complementarymetal oxide semiconductor(CMOS) - electron or hole current.

Note: The terms MOS and CMOS are another type of transistor and the trainees are requested to refer any standard electronic book for further reference.

ICs are available in different packages and shapes. The usual packages are:

- dual in the packages DIP
- single in line package SIP and
- metal can packages.

ICs handling power more than IW are provided with heat sinks.

Advantages of integrated circuits over discrete circuit (Refer Table 1)

Table 1


When the advantages are considered, the disadvantages of IC are negligible. They are widely used for different applications such as voltage regulators, audio amplifiers, TV circuits, computers, industrial amplifiers etc. ICs are available in different pin configurations in different outlines suitable for different circuits.

Integrated circuit (IC) voltage regulators: The series voltage regulators discussed in earlier lessons are available in the form of integrated circuits (ICs). They are known as voltage regulator ICs.

There are two types of voltage regulator ICs. They are,

- Fixed output voltage regulator ICs
- Adjustable output voltage regulator ICs.

Fixed output voltage regulator ICs: The latest generation of fixed output voltage regulator ICs have only three pins as in Fig 1. They are designed to provide either positive or negative regulated DC output voltage.


These ICs consist of all those components and even more in the small packages in Fig 1. These ICs, when used as voltage regulators, do not need extra components other than two small value capacitors as in Fig 2.


The reason behind using capacitor $\mathrm{C}_{1}$ is when the voltage regulator IC is more than a few inches from the filter capacitors of the unregulated power supply, the lead inductance may produce oscillations within the IC. Capacitor $C_{1}$ prevents setting up of such oscillations. Typical value of bypass capacitor $\mathrm{C}_{1}$ range from $0.220 \mu \mathrm{~F}$ to $1 \mu \mathrm{~F}$. It is important to note that $\mathrm{C}_{1}$ should be connected as close to the IC as possible.

The capacitor $\mathrm{C}_{2}$ is used to improve the transient response of the regulated output voltage. $\mathrm{C}_{2}$ bypasses these transients produced during the ON/OFF time. Typical values of $C_{2}$ range from $0.1 \mu \mathrm{~F}$ to $10 \mu \mathrm{~F}$.

Fixed voltage three terminal regulators are available from different IC manufacturers for different output voltages (such as $5 \mathrm{~V}, 9 \mathrm{v}, 12 \mathrm{~V}, 24 \mathrm{~V}$ ) with maximum load current rating ranging from 100 mA to more than three amps.

The most popular three terminal IC regulators are,
1 LMXXX-Xseries
Example: LM320-5, LM320-24 etc.
2 78XXand79XX series
Example: 7805, 7812, 7912 etc.
A list of popular three terminal regulators is given in IC data book.

Specifications of three terminal IC regulators: For simplicity in understanding, let us consider the specification of a three terminal IC $\mu \mathrm{A} 7812$. The table 2 given below lists the specifications of $\mu \mathrm{A} 7812$.

Table 2

| Parameter | Min. | Type. | Max. | Units |
| :--- | :--- | :--- | :--- | :--- |
| Output voltage | 11.5 | 12 | 12.5 | V |
| Output regulation |  | 4 | 120 | mV |
| Short-circuit <br> output current <br> Drop out voltage <br> Ripple rejection | 55 | 71 |  | 350 |
| Peak output <br> current |  | 2.2 |  | mA |

Output voltage: This specification indicates the regulated DC output voltage that can be obtained from the IC. As can be seen from the sample specification table given above, the manufacturer specifies minimum, typical and maximum output voltage. While using this IC take the typical value as this value corresponds to the output voltage at IC under normal input and load conditions.

Output regulation: This indicates the amount by which the output voltage may vary at rated maximum load condition. For example, in $\mu$ A7812 IC, the output voltage may vary by 4 mV from its rated 12 V DC when the rated typical load current is 2.2A.

Short circuit output current: This indicates the shorted current $I_{s c}$, if the output gets shorted. In $\mu \mathrm{A} 7812$ the output current is limited to 350 mA when the output terminals are shorted.

These regulators also canbe used fold back current limiting.

Drop out voltage: For instance, in $\mu \mathrm{A} 7812$ in which the output voltage is +12 V , the input unregulated DC voltage to the regulator must be higher than the output voltage. The specification drop out voltage indicates, the minimum positive different between the input and output voltages for the IC to operate as a regulator. For example, in, $\mu \mathrm{A} 7812$ the unregulated input voltage should be atleast 2 volts more than the regulated $D C$ output of 12 V . This means for $\mu \mathrm{A} 7812$ the input must be atleast 14 V .

The difference between the voltage across the input and output of the IC should also not to be very high as this causes unwanted dissipation. As a thumb rule, the input voltage to the regulator shall be restricted to a maximum of twice the output voltage of the regulator. For example, for $\mu \mathrm{A} 7812$, the unregulated input voltage should be more than 14 V , but less than 24 V .

- Ripple rejection

This indicates the ratio of ripple rejection between the output to input, expressed in decibels,

## - Peak output current

This indicates the highest output or load current that can be drawn. Above this rated maximum current the safety of the IC is not guaranteed.

Identification of output voltage and rated maximum load current from IC type number

- 78XXand79XX series are3Terminal voltage regulators.
- All 78XX series are positive output voltage regulators
- All 79XX series are negative output voltage regulators

The term XX indicates the rated output regulated voltage.

## Example



It is important to note that, different manufacturers of 78 XX/ 79XX series such as Fair Child (MA/Mpc), Motorola, Signetics (SS) adopt slightly different coding schemes to indicate the rated maximum current of the three pin regulated. ICs. One such scheme is given below.

| 78LXX | - | L indicates rated maximum load <br> current as 100 mA. |
| :--- | :--- | :--- |
| $78 \mathrm{MXX}-$ | M indicates rated a maximum load <br> current as 500 mA |  |
| 78 XX | - | Absence of an alphabet between 78 <br> and $X X$ indicates that the rated <br> maximum load current is 1A. | current as 100 mA . maximum load current is 1 A .

78SXX - S indicates rated maximum load current is 2amp.

## Example



LM 3XX series of 3 terminal voltage regulators: In LM series of three terminal regulators, to find the specifications, it is suggested to refer to its data manual. However, the following tips will help in identifying whether the IC is a fixed positive or fixed negative regulator.

| LM320-X andLM320-XX $\rightarrow$Fixed-ve voltage <br> regulators. |  |
| ---: | :--- |
| LM340-XorLM340-XX $\rightarrow$ | Fixed +ve voltage <br> regulators. |

## Examples



Practical 78XX and 79XX voltage regulator: Fig 3 shows the circuit connections of a $12 \mathrm{~V}, 1 \mathrm{~A}$ regulated power supply using 7812.


The output voltage of a 3-terminal regulator IC is with reference to the IC's common terminal (COM). When the COM terminal is grounded, the output voltage of the regulator will be the specified output voltage of the IC as in Fig 3. But the output voltage of the IC can be increased above the specified value by rising the voltage at the COM terminal as in Fig 4. Because of 6.1 V zener, the output voltage of the IC can be increased above the specified value by raising the voltage at the COM terminals
as in Fig 4. Because of 6.1 V zener, the output voltage will be $6.1 \mathrm{~V}+12 \mathrm{~V}=18.1 \mathrm{~V}$ or approximately 18 V as in Fig 4.


When the COM terminal of the IC is grounded as in Fig 2, the quiescent current flowing from the COM terminal to ground in 78 series is around $8 \mu \mathrm{~A}$. This current decreases as the load current increases. When a zener is connected at COM terminal as in Fig 4, to ensure that the zener is always in the reverse $O N$ condition, resistor $R_{1}$ is used. If $R_{1}=1.8 \mathrm{~K}, I_{z}$ will be 7 mA which is sufficient to keep the zener ON always.

Fig 5 shows a variable output voltage regulator. The variable reference voltage at COM terminal is obtained using a POT.


Four-terminal regulators: These are adjustable output voltage regulators and are also available as +ve and -ve regulators. These ICs have internal reference voltages and are protected internally for thermal overload, short circuit etc. Table 1 provides important specifications for most common ICs.

Fig 6 to 8 shows the common ICs used as voltage regulators with their terminal marking and Fig 9 to 11 shows the circuit configuration.


Fig 7


Fig 8


IN

Fig 9


Fig 10


ELN411721A

Fig 11


Table 3

## Specifications of a 4-terminal voltage regulator

| SI. No. | IC | MA 78G | MA78MG | MA79G | MA79MG |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | Input voltage range | 7.5 V to 40 V | 7.5 V to 40 V | -7 V to -40 V | -7 V to -40 V |
| 2 | Output voltage range | 5 V to 30 V | 5 V to 30 V | -2.23 V to -30 V | -2.23 V to -30 V |
| 3 | Line regulation | 4 | - better th | \% for all | $\longrightarrow$ |
| 4 | Load regulation |  | better | 1\% for all | , |
| 5 | Drop out voltage | 3 V | 3 V | 2.5 V | 2.5 V |
| 6 | Peak output current | 2.2A | 800 mA | 2.2A | -800mA |
| 7 | Control pin current | $5 \mu \mathrm{~A}$ | $5 \mu \mathrm{~A}$ | $2 \mu \mathrm{~A}$ | $2 \mu \mathrm{~A}$ |
| 8 | Short circuit current | 750 mA | 300 mA | 250 mA | 100 mA |
| 9 | Internal reference voltage | 5 V | 5 V | 2.23 V | 2.23 V |
| 10 | Ripple reflection \{When the $\left.\left[\left(\mathrm{V}_{\text {IN }}\right)-\left(\mathrm{V}_{\text {OUT }}\right)\right]>10 \mathrm{~V}\right\}$ |  |  | 1000 | $\longrightarrow$ |

## Binary numbers, logic gates and combinational circuits

Objectives : At the end this lesson you shall be able to

- explain the digital electronics principle and positional notation and weightage
- explain decimal to binary conversion, binary odometer
- explain hexadecimal number system
- convert decimal to hexa, hexa to decimal and BCD system
- explain logic gates principle - NOT, OR and AND gates with truth table
- explain combinational gates - NAND, NOR with truth table and logic pulser.


## Introduction

When we hear the word 'number' immediately we recall the decimal digits $0,1,2 \ldots .9$ and their combinations. Digital circuits do not process decimal numbers. Instead, they work with binary numbers which use the digits ' 0 ' and ' 1 ' only. The binary number system and digital codes are fundamental to digital electronics. But people do not like working with binary numbers because they are very long when representing larger decimal quantities. Therefore digital codes like octal, hexadecimal and binary coded decimal are widely used to compress long strings of binary numbers.

Binary number systems consists of 1 s and 0 s . Hence this number system is well suited for adopting it to the digital electronics.

The decimal number system is the most commonly used number system in the world. It uses 10 different characters to show the values of numbers. Because this number system uses 10 different characters it is called base-10 system. The base of a number system tells you how many different characters are used. The mathematical term for the base of a number system is radix.

The 10 characters used in the decimal number systems are $0,1,2,3,4,5,6,7,8,9$.

## Positional notation and weightage

A decimal integer value can be expressed in units, tens, hundreds, thousands and so on. For example decimal number 1967 can be written as $1967=1000+900+60+$ 7. In powers of 10, this becomes.

|  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $10^{3}$ | $10^{2}$ | $10^{1}$ | $10^{0}$ | $1 \times 10^{3}=$ | 1000 |
| $9 \times 10^{2}=$ | 900 |  |  |  |  |
| $6 \times 10^{1}=$ | 60 |  |  |  |  |
| 1 | 9 | 6 | 7 |  | $7 \times 10^{\circ}=$ |
|  |  |  |  |  | 7 |

i.e. $[1967]_{10}=1\left(10^{3}\right)+9\left(10^{2}\right)+6\left(10^{1}\right)+7\left(10^{0}\right)$

This decimal number system is an example of positional notation. Each digit position has a weightage. The positional weightage for each digit varies in the sequence $10^{\circ}, 10^{1}$, $10^{2}, 10^{3}$ etc starting from the least significant digit.

The sum of the digits multiplied by their weightage gives the total amount being represented as shown above.

In a similar way, binary number can be written in terms of weightage.

Toget the decimal equivalent, then the positional weightage should be written as follows.

$$
\begin{aligned}
{[1010]_{2} } & =1\left(2^{3}\right)+0\left(2^{2}\right)+1\left(2^{1}\right)+0\left(2^{0}\right) \\
& =8+0+2+0 \\
{[1010]_{2} } & =[10]_{10}
\end{aligned}
$$

Any binary number can be converted into decimal number by the above said positional weightage method.

## Decimal to Binary conversion

Divide the given decimal number by 2 as shown below and note down the remainder till you get the quotient - zero.

## Example

|  | 0 |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| 2 | 1 | 1 | $\longrightarrow$ |  |
| 2 | 2 | 0 |  |  |
| 2 | 4 | 0 |  |  |
| 2 | 8 | 0 |  |  |
| 2 | 17 | 1 |  |  |
| 2 | 34 | 0 | $\longrightarrow$ |  |

The remainder generated by each division form the binary number. The first remainder becomes the LSB and the last remainder becomes the MSB of binary number.

Therefore, $[34]_{10}=[100010]_{2}$

## Counting binary number

To understand how to count with binary numbers, let us see how an odometer (KM indicator of a car) counts with decimal numbers,

The odometer of a new car starts with the reading 0000.
After traveling 1KM , reading becomes 0001.
Successive KM produces 0002, 0003 and so on upto 0009
At the end of 10 th KM , the units wheel turns back from 9 to 0 , a tab on this wheel forces the tens wheel to advance by 1 . That is why the number changed from 0009 to 0010. That is, the units wheel is reset to 0 and sent a carry to the tens wheel. Let us call this familiar action as reset and carry. The other wheels of odometer also reset and carry. For instance, after covering 999KM , the odometer shows 0999.

After the next KM , the unit wheel resets and carries, the tens wheel resets and carries, the hundreds wheel resets and carries and the thousands wheel advances by 1 to get the reading 01000.

## Binary odometer

Visualize a binary odometer, a device whose wheels have only two digits 0 and 1. When each wheel turns, it displays 0 then 1 and then back to 0 and the cycle repeats. A four digit binary odometer starts with 0000.

After 1 km , it indicates - 0001 .
The next km forces the units wheel to reset and sends carry. So the number changes to 0010.

The third km results in 0011.
After 4 km , the units wheel resets and sends carry, the second wheel resets and sends carry and the third wheel advances by 1 . Hence it indicates 0100.

Table below shows all the binary numbers from 0000 to 1111 equivalent to decimal 0 to 15.

| Decimal | Binary |
| :---: | :---: |
| 0 | 0000 |
| 1 | 0001 |
| 2 | 0010 |
| 3 | 0011 |
| 4 | 0100 |
| 5 | 0101 |
| 6 | 0110 |
| 7 | 0111 |
| 9 | 1000 |


| Decimal | Binary |
| :---: | :---: |
| 10 | 1010 |
| 11 | 1011 |
| 12 | 1100 |
| 13 | 1101 |
| 14 | 1110 |
| 15 | 1111 |

Addition of binary numbers

Sum
$0+0=0$
$1+0=1$
$0+1=1$
$1+1=0$

Ex: 1
Ex: 2
10

+ 11
$1+1+1=1$
$+1$
(Oneplusoneplus one is equal toone with carry one)
$\qquad$
101
11

Hexadecimal number system: In hexadecimal system there are 16 characters. They are $0,1,2,3,4,5,6,7,8,9$, $A, B, C, D, E, F$ where $A=10, B=11, C=12, D=13, E=14$, $\mathrm{F}=15$ in decimal. In this system, the base is 16 . This system is mainly used to develop programmes for computers.

## For Example

$$
\begin{aligned}
& {[23]_{16}=[35]_{10} ; 16^{1} \times 2+16^{0} \times 3=32+3=35} \\
& {[2 \mathrm{C}]_{16}=[44]_{10} ; 16^{1} \times 2+16^{0} \times 12=32+12=44}
\end{aligned}
$$

## Decimal to hexadecimal conversions

The conversion of decimal to hexadecimal is similar to binary conversion. Only difference is that divide the decimal number successively by 16 , and note down the remainder.

|  | 0 |  |
| :---: | :---: | :---: |
| 16 | 1 | $1 \longrightarrow$ MSB |
| 16 | 27 | 11 or B |
| 16 | 432 | $0 \longrightarrow$ LSB |
| $[432]_{10}=[1 \mathrm{B0}]$ |  |  |

## Hexadecimal to Decimal

This conversion can be done by putting it into the positional notation.

$$
\text { Ex: } \begin{aligned}
223 A_{16} & =2 \times 16^{3}+2 \times 16^{2}+3 \times 16^{1}+A \times 16^{0} \\
& =2 \times 4096+2 \times 256+3 \times 16+10 \times 1 \\
& =8192+512+48+10 \\
& =8762_{10}
\end{aligned}
$$

## BCD (Binary Coded Decimal)

Binary Coded Decimal (BCD) is a way to express each of the decimal digits with a binary code, since there are only ten code groups in the BCD system, it is very easy to convert between decimal and BCD. Because decimal system is used for read and write, BCD code provides an excellent interface to binary systems. Examples of such interfaces are keypad inputs and digital readouts.

## 8421 code

The 8421 code is a type of binary coded decimal (BCD), binary coded decimal means that each decimal digit, 0 through 9 is represented by a binary code of four bits. The designation 8421 indicates the binary weights of the four bits $\left(2^{3}, 2^{2}, 2^{1}, 2^{0}\right)$. The ease of conversion between 8421 code numbers and the familiar decimal numbers is the main advantage of this code. All you have to remember are the ten binary combinations that represents the ten decimal digits as shown in the Table.

| Decimal <br> digit | 0 | 1 | 2 | 3 | 4 |
| :--- | :--- | :--- | :--- | :--- | :---: |
| BCD | 0000 | 0001 | 0010 | 0011 | 0100 |
| Decimal <br> digit | 5 | 6 | 7 | 8 | 9 |
| BCD | 0101 | 0110 | 0111 | 1000 | 1001 |

The 8421 code is the pre-dominant BCD code, and when we refer to BCD, we always mean the 8421 code unless otherwise stated.

## Inverters (NOT Gate)

An inverter is a gate with only one input signal and one output signal. The output state is always the opposite of the input state. Logic symbol is shown in Fig 1.


## Transistor inverter

The Fig 2 shows the transistor inverter circuit. The circuit is a common emitter amplifier which works in saturation or in cut off region depending upon the input voltage. When $\mathrm{V}_{\text {in }}$ is in low level, say less than the transistor cut in voltage 0.6 V in silicon type, the transistor goes to cut off condition and the collector current is zero. Therefore, $\mathrm{V}_{\text {out }}=+5 \mathrm{~V}$ which is taken as high logic level. On the other hand, when $\mathrm{V}_{\text {in }}$ is in high level, the transistor saturates and $\mathrm{V}_{\text {out }}=\mathrm{V}_{\text {sat }}$ $=0.3 \mathrm{~V}$ i.e low level.


The table summarizes the operation

| $\mathbf{V}_{\text {in }}$ | $\mathbf{V}_{\text {out }}$ |
| :--- | :--- |
| Low(0) | $\operatorname{High}(1)$ |
| High(1) | $\operatorname{Low(0)}$ |

The logic expression for the inverter is as follows: Let the input variable be ' $A$ ' and the output variable be $Y$, then the output $\mathrm{Y}=\overline{\mathrm{A}}$.

## OR and AND gate circuits

## OR Gate

The output of an OR will be in 1 state if one or more of the inputs is in 1 state. Only when all the inputs are in 0-state, the output will go to 0 -state. Fig 3 shows the schematic Symbol of an OR Gate :

## Fig 3



The boolean expression for $O R$ gate is $Y=A+B$.
The equation is to be read as $Y$ equals $A$ ORed $B$. Twoinput truth table given below is equivalent to the definition of the OR operation.

Truth table for OR gate

| $A$ | $B$ | $Y=A+B$ |
| :--- | :--- | :--- |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |

## Electrical equivalent circuit

The Fig 4a shows the electrical equivalent circuit of an OR gate. It is evident that if any one of the switch is closed, there will be output.

## 2 in-put OR gate using diode

The Fig 4b shows one way to build a 2 -input OR gate, using diodes. The inputs are labeled as $A$ and $B$, while the output is Y .

Fig 4


$$
\begin{array}{ll}
\text { Assume } & \text { logic } 0=0 \mathrm{~V} \text { (low) } \\
& \text { logic } 1=+5 \mathrm{~V} \text { (high) }
\end{array}
$$

Since this is a 2 input OR gate, there are only four possible cases,

Case 1: $A$ is low and $B$ is low. With both the input voltage low, both the diodes are not conducting. Therefore the output Y is in low level.

Case 2: $A$ is low and $B$ is high, The high $B$ input voltage $(+5 \mathrm{~V})$ forward biases the lower diode, producing an output voltage that is ideally +5 V (actually +4.3 V taking the diode voltage drop 0.7 V into consideration). That is, the output is in high level. During this condition, the diode connected to input $A$ is under reverse bias or OFF condition.

Case 3: $A$ is high and $B$ is low, the condition is similar to case 2. Input A diode is ON and Input B diode is OFF and $Y$ is in high level.

Case 4: $A$ is high, $B$ is high. With both the inputs at +5 V , both diodes are forward biased, since the input voltages are in parallel, the output voltage is +5 V ideally $[+4.3 \mathrm{~V}$ to a second approximation]. That is, the output Y -is in high level.

OR gates are available in the IC form. IC7432 is a T.T.LOR gate IC having 4 OR gates inside it.

## Simple application of OR gate

## Intrusion detection

Simplified portion of an intrusion detection and alarm system is two windows and a door. The sensors are magnetic switches that produce a high(1) output when windows and doors are opened and a low(0) output when closed. As long as the windows and the door are secured, the switches are closed and all three of the OR gate inputs are in low(0). When one of the windows or the door is opened, a high(1) output is produced on that input of the OR gate and the gate output goes high. It then activities an alarm circuit to warn of the intrusion.

## AND gates

The AND gate has two or more inputs but only one output. All input signals must be held high to get a high output.

Even if one of the inputs is low, the output becomes low.
AND gate symbols for 2 input and 3 input gates are shown in Fig 5a and 5b.


Truth table
Two input AND gate

| $A$ | $B$ | $Y=A B$ |
| :--- | :--- | :--- |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Three input AND GATE

| $A$ | $B$ | $C$ | $Y=A B C$ |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

## Electrical equivalent circuit of an AND gate

The output is available only when both the switches are closed. IC7408 is a T.T.L quad AND gate IC. (Refer data book for pin diagram). The electrical equivalent of AND gate and AND gate using diodes are shown in Fig 6a and 6 b.

Fig 6
(a)

(b)


## Two input AND gate using diode

## I condition

$A=0, B=0, Y=0$ as in Fig 7 .


During the above condition I/P A and B are connected to ground to make logic low inputs. During this condition, both the diodes conduct, and pulls the O/P Y to logic-0.

## II condition

$A=0, B=1, Y=0$ as in Fig 8.


In the II condition shown in the figure above, diode $D_{1}$ is connected logic-0 input and diode $\mathrm{D}_{2}$ is connected to +5 V [Logic high]. Diode $D_{1}$ is in forward bias and conducts. Diode $D_{2}$ is having equal potential $(+5 \mathrm{~V})$ at anode and cathode. So potential difference between anode and cathode is 0 . Hence diode D2 does not conduct. The output $Y$ is pulled down to logic zero, since $D_{1}$ is conducting.

## III condition

$A=1, B=0, Y=0$ as in Fig 9.


The III condition is similar to the II condition. $\mathrm{D}_{2}$ is forward biased. $D_{1}$ is reverse biased. Hence output $Y$ is pulled to logic-0.

## IV condition

$\mathrm{A}=1, \mathrm{~B}=1, \mathrm{Y}=1$ as in Fig 10 .


In this condition both the diodes are reverse biased. So both the diodes act as open circuit. Therefore output $y$ is +5 V i.e y is in logic-1 condition.

## AND gate as an Enable/Inhibit device

A common application of the AND gate is to enable (i.e to allow) the passage of a signal (pulse waveform) from one point to another at certain times and to inhibit (prevent) the passage at other times.

In Fig 11a AND gate controls the passage of a signal (waveform A) to a digital counter. The purpose of this circuit is to measure the frequency of waveform ' $A$ '. The enable pulse has a width of precisely 1 second. When the enable pulse applied at $B$ is high, waveform $A$ passes through the gate to the counter, and when the enabled pulse is low, the signal is prevented (inhibited) from passing through. Refer Fig 11b for the waveforms of the above process.


During the 1 second interval of the enabled pulse, a certain number of pulses in waveform A pass through the AND gate to the counter. The number of pulses counted by the counter is equal to the frequency of the waveform A. For example, if 1000 pulses pass through the gate in the 1 second interval of the enabled pulse, there are 1000 pulses $/ \mathrm{sec}$. That is, frequency is 1000 Hz .

## Combinational gate circuits - NOR and NAND

## NOR Gate

In Fig 12a the output $y$ of the circuit equals to the complement of A OR B, because the circuit is an OR gate followed by a NOT gate. To obtain high output [Logic-1], both the inputs should be tied to low input [Logic-0]. For the rest of the other three possibilities, output will be zero, the combination of this OR and NOT gate is called as NOR gate.

Fig 12(a)


Symbol (Fig 12b) :

Fig 12(b)

We can define a NOR gate as follows:
The output of a NOR gate is 0 , even if one of the inputs is in logic-1. Only when both the inputs are in logic-0, the output is in logic-1.

## Truth table

| $A$ | $B$ | $A+B$ |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

IC7402 is a T.T.L NOR gate IC. It contains 4 NOR gates. For pin details, refer data book.

## NAND gate

An AND gate followed by a NOT gate forms the NAND gate as in Fig 13a. In this gate to get a low output (logic=0), all the inputs must be in high state and to get high output state, any one of the inputs or both inputs must be in low state.

Fig 13
(a)

(b)


Fig 13b is the standard symbol for a NAND gate. The inverter triangle has been deleted and the bubble is moved to the AND-gate output.

Truth table for NAND gate

| $A$ | $B$ | $Y=\overline{A B}$ |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## Pulsed operation

Output waveform Y is low only for the time intervals when both inputs $A$ and $B$ are high as shown in the timing diagram Fig 14.

## Logic pulser

Fig 15 shows the circuit diagram of logic pulser, the circuit essentially consists of NAND gates connected debouncer circuit and its outputis Double inverted. The LED indicates, pulses ON or OFF status.


When switch $S_{1}$ is not pressed, (OFF position) $B$ input of NAND gate No. 2 is grounded, hence its output $\bar{Y}$ isforced to go logic HIGH. This HIGH output is feedback to NAND gate 1 , A input of NAND gate 1 is also held HIGH through $\mathrm{R}_{1}$ resistor (820 $\Omega$ ) and thus the output of NAND gate-1 ' Y ' is at low. This logic low output keeps LED in OFF condition and this logic low is again double inverted at the logic pulser tip through NAND gate 3 and 4 to get logic low level at pulser tip.

When $\mathrm{S}_{1}$ is pressed to ON, A input of NAND gate is forced to go logic-low. Hence the output of this NAND gate is forced to go logic-HIGH. Therefore the 'Y' output is at logic1, so LED glows and a logic-HIGH appears at probe tip. Also note that with HIGH at Y output, the inputs of NAND gate 2 are also at logic-HIGH and the output of NAND gate-2 is forced to go low. As long as switch $\mathrm{S}_{1}$ is at ON position the probe tip is HIGH. When it is released it springs back to OFF position, and the output returns to a logic-LOW condition.

## Electrician - Electronic Practice

## Wave shapes - oscillators and multivibrators

Objectives: At the end of this lesson you shall be able to

- state the working principle and gain of oscillator
- explain the RC phase-shift oscillator and frequency calculation
- state the features, gain and frequency of Hartley, colpitts and crystal oscillators
- state the working principle and frequency calculation of bistable and monostable multivibrator using CRO.

Oscillator: An oscillator is a circuit for producing voltages that vary in a regular fashion with respect to time. The output wave forms of oscillators are repeated exactly in equal successive intervals of time as in Fig 1a and Fig 1b.


The output wave-form of an oscillator may be sinusoidal as in Fig 1a. Such oscillators are known as sine wave oscillators or harmonic oscillators.

The output of oscillators may be square, triangular or sawtooth wave forms as in Fig 1b. Such oscillators are known as non-sinusoidal oscillators or relaxation oscillators.

It was discussed earlier that positive feedback results in converting an amplifier into an oscillator. To provide positive feedback the feedback signal should be inphase with the input signal such that it adds up with the input signal.

In practice, an oscillator will have no input AC signal at all, but it still generates AC signal. An oscillator will have only a DC supply. The oscillator circuit, makes use of the noise generated in resistors at the switching on time of dc supply and sustains the oscillations.

To build an oscillator, the following are essential;

- An amplifier
- A circuit which provides positive feedback from output to input.
The gain of an amplifier with feedback is given by,

$$
A_{v f}=\frac{A_{V}}{1-k A_{V}}
$$

$k A_{v}$ is known as the loop gain of the amplifier. In the case of the amplifiers when the sign associated with $k A_{v}$ is negative, the denominator has value more than 1. And, hence the value of Avt will always be less than $A_{v}$ (negative feedback). But, if the value of $k A_{v}$ is made larger, such that, it approaches unity, and, if the sign associated with $k A_{v}$ is negative then the value of the denominator decreases to less than 1 , and hence, $A_{v f}$ will be larger than $A_{v}$.

In case of oscillators, if the loop gain $k A_{v}$ is made positive, i.e. by feeding back signal which is in-phase with the input signal, then there will be an output signal even though there is no external input signal. In other words, an amplifier is modified to be an oscillator by positive feedback such that it supplies its own input signal.

## Example

An amplifier has a voltage gain of 40 without feedback. Determine the voltage gains when positive feedback of the following amounts is applied.
i) $\mathrm{k}=0.01$
ii) $k=0.02$
iii) $k=0.025$

## Solution

i) $A_{v f}=\frac{A_{V}}{1-k A_{V}}=\frac{40}{1-0.01 \times 40}=\frac{40}{0.6}=66.7$
ii) $A_{v f}=\frac{A_{V}}{1-k A_{V}}=\frac{40}{1-0.02 \times 40}=\frac{40}{0.2}=200$
(iii) $\quad A_{\mathrm{Vf}}=\frac{\mathrm{A}_{\mathrm{V}}}{1-\mathrm{kA}}=\frac{40}{1-0.025 \times 40}=\frac{40}{0}=\infty$ (Infinity)

In (iii) the gain of the amplifier become infinite when the loop gain $k A_{v}=+1$. This is known as the critical value of the loop gain $k A_{v}$. It is important to note that the output voltage cannot be infinite. Instead the amplifier will start working as an oscillator without the need of any separate input. If the feedback path contains a frequency selective network, the requirement of $k A_{v}=1$ can be met at only one particular frequency, such that, the output of the oscillator will be a sinusoidal signal of a particular frequency. Such oscillators are known as sine wave oscillators.

One of the simplest form of sine wave oscillators is the phase shift oscillator. Fig 2 shows the principle behind an RC phase shift oscillator.

Fig 2


The feedback network shown in Fig 3 consists of resistors and capacitors which provide the required phase shift of $180^{\circ}$. Due to the presence of capacitors in the feedback network, the feedback network can be so designed to provides the required phase shift of exactly $180^{\circ}$ at a particular frequency f given by,


$$
f=\frac{1}{2 \pi R C \sqrt{6}}
$$

The other condition to be satisfied oscillations to occur is that the loop gain $\mathrm{KA}_{\mathrm{v}}$ should be equal to unity. To satisfy this condition, using classical network analysis, it can be found that, the value of $K$ should be, $k=1 / 29$. Therefore, the voltage gain of the amplifier $\mathrm{A}_{\mathrm{v}}$ stage must be greater than $1 / k$ or greater than 29 so that $k A_{v}$ becomes equal to 1.

Transistor RC phase shift oscillator: Fig 3 shows a single transistor phase shift oscillator using resistors and capacitors in a feedback network.

There are three sections of $R$ and $C$ in the feedback network. Each RC section provides a $60^{\circ}$ phase shift at a specific frequency, resulting in a $180^{\circ}$ phase shift as required for positive feedback. This satisfies one of the two required conditions for oscillations.

In Fig 3, the feedback signals coupled through a feedback resistor $R^{1}$ in series with the amplifier stage input Resistance $R_{\text {in }}$. resistor $R^{1}$ can be made variable for adjusting the oscillator frequency. For each of three sections of $R_{c}$ phase shift network to produce $60^{\circ}$ phase shift, it is necessary that $\mathrm{C}_{1}=\mathrm{C}_{2}=\mathrm{C}_{3}$ and $\mathrm{R}_{1}=\mathrm{R}_{2}=\mathrm{R}^{\prime}+\mathrm{R}_{\text {in }}$.

The other required condition for oscillation, i.e. loop gain $k A_{v}$ to be unity is satisfied by the circuit at Fig 2, when $\beta$ of the transistor used in the circuit is,
$\mathrm{h}_{\mathrm{fe}}=\beta=23+29 \frac{\mathrm{R}}{\mathrm{R}_{\mathrm{C}}}=+4 \frac{\mathrm{R}_{\mathrm{C}}}{\mathrm{R}}$
where, $\mathrm{R}_{1}=\mathrm{R}_{2}=\mathrm{R}$
When $\beta$ is atleast the value given by equation (2) or greater than, the circuit at Fig 2 it will oscillate.

## Practical transistor RC phase shift oscillator

Fig 4 shows a practical transistor RC phase shift oscillator which is similar to that shown in Fig 2.

In Fig 4 note that resistor $R_{3}$ (in Fig 2 it is denoted as $\mathrm{R}^{\prime}$ ) used for frequency adjustments is connected in series with one of the resistors of the RC section. Resistor $R_{4}$ provides the necessary bias stabilisation for the transistor operation. Note that a small value capacitor $\mathrm{C}_{4}$ is connected in parallel with the input. The purpose of $\mathrm{C}_{4}$ is to bypass the unwanted high frequency oscillations to ground. The value of $R_{3}$ can be varied to adjust the frequency of oscillations. However, the variation that can be obtained by $R_{3}$ is limited.

For the circuit at Fig 3, the frequency of oscillation is given by,


$$
\begin{equation*}
\mathrm{f}=\frac{1}{2 \pi \mathrm{C} \sqrt{6 \mathrm{R}_{1}{ }^{2}+4 \mathrm{R}_{1} \mathrm{R}_{\mathrm{C}}}} \tag{3}
\end{equation*}
$$

where, $C=C_{1}=C_{2}=C_{3}$
The minimum value of hfe or $\beta$ of the transistor used in the circuit at Fig 3 should be,

$$
\mathrm{h}_{\mathrm{fe}}=\beta=23+29 \frac{\mathrm{R}_{1}}{\mathrm{R}_{\mathrm{C}}}+4 \frac{\mathrm{R}_{\mathrm{C}}}{\mathrm{R} 1}
$$

using the component values at Fig 3 , the $\beta$ of the transistor used should be a minimum of,

$$
\beta=23+29 \frac{1.2 \mathrm{~K}}{5.6 \mathrm{~K}}+4 \frac{5.6 \mathrm{~K}}{1.2 \mathrm{~K}}=47.89
$$

> The frequency of oscillations can be increased by decreasing the value of $R$ or by decreasing the value of $C$.

In the practical circuit at Fig 3, collector feedback bias is employed to ensure that the transistor will never go to saturation. Other biasing techniques such as voltage divider bias can also be used for DC biasing of the transistor. Since the frequency of oscillations is decided only by the feedback phase shift network, biasing resistors will nothave any effect of the frequency of oscillations. The important point to be noted is that the $\beta$ of the transistor should be higher than the minimum $\beta$ given in equation 2 to have sustained oscillations.

## Hartley oscillator

Principle of sinusoidal or harmonic oscillations: Fig 5 a shows an inductor and a capacitor connected in parallel as a parallel LC resonant circuit. A parallel LC circuit is also known as tuned circuit or tank circuit.

In Fig 5a, when switch $S$ is put into position $A$, the capacitor gets charged with the bottom plate being negative and the top plate positive. This means, energy is stored in the capacitor in the form of an electric charge.

When switch $S$ is put into position $B$, as in Fig 5b, the capacitor starts discharging through the inductor, creating an expanding magnetic field around L . Since the inductor has the property of opposing any sudden change in current through it, the current builds up slowly.

Once the capacitor gets fully discharged, the magnetic field around L begins to collapse. The collapsing magnetic field, induces a voltage (back-emf) in L. This back emf tends to maintain the electron flow through $L$ in the same direction as when C was discharging. Hence, this back emf in the inductor starts charging the capacitor with opposite polarity as in Fig 5c. After the magnetic field has totally collapsed, C would have got charged in the opposite direction as in Fig 5c.

Sinusoidal wave form: However, owing to the resistance in a practical inductor and the losses in the capacitor due to resulting $I^{2} R$ (heat loss) the amplified of the oscillation decreases gradually (damped) and ultimately the oscillations die down as in Fig 5d.


The frequency of oscillation produced by the resonant frequency is given by,

$$
f=\frac{1}{2 \pi \sqrt{L C}}
$$

Overcoming losses in tank circuit for sustained oscillations: To avoid the damping of oscillations, when the energy fed into the circuit has been used up, it is necessary to supply more energy by charging the capacitor again. As shown in Fig 5a, by switching $S$ between $A$ and $B$ at proper time, the oscillations can be maintained thus obtaining sinusoidal waveform of constant amplitude and frequency.

Another method of making the LC tank circuit to give undamped oscillations is, to connect the tank circuit in the output of an amplifier as in Fig 6.


The amplifier is kept at cut-off by the dc supply $\mathrm{V}_{\mathrm{BB}}$ which reverse-biases the base-emitter circuit. A sine wave is injected to the base circuit with such an amplitude that the collector current flows at the peak of the negative alterations of the input sine wave. This excites the LC circuit in the collector of the transistor and the tank keeps oscillating. If the input sine wave has the same frequency as the frequency of oscillations of the tank circuit, the oscillations in the LC tank is maintained.

Fig 7 shows a modified form of circuit at Fig 6. In Fig 5a transistor amplifier connected in such a way that it will cause undamped oscillations without requiring any external signal. Such a circuit is known as an oscillator.


The oscillator circuit at Fig 7 is known as tickler-coil oscillator. Here L1 is inductively coupled to L. When power is first switched ON to the circuit, current flows in the transistor. As the current flows through $L$, it induces a voltage in L1 which is coupled to the base of the transistor and is amplified.

If the phase of the feedback voltage is adding, then there is an increase in the collector current. This action builds up a large current pulse which excites the LC tank into oscillations. The signal fed by L1 to the base of the transistor is a sine wave of the same frequency as that in the LC circuit and of proper phase to sustain the oscillations.

The signal induced in the base thus eliminates the need for an external input to the oscillator and the LC tank will oscillate as long as the DC power to the circuit is ON.

The feedback given to the amplifier in Fig 7 in the proper phase so as to sustain (keep going) oscillations is referred to as positive feedback or regenerative feedback.

Barkhausen criterion: The mathematical analysis for an amplifier to oscillate on its own is given below:

- In the amplifier shown in Fig 7, assume that the gain of the amplifier is $A$ and the feedback factors is $\beta$. If the product of $A \beta$ is less than $1(A \beta<1)$, then the output signal will be a damped oscillations which will die down as is shown in Fig 8a.
- If $A \beta>1$, the output voltage builds up as shown in Fig 8b. Such oscillations are called growing oscillations.
- If $A \beta=1$, the output amplitude of oscillations remains constant as in Fig 8c.


When the feedback is positive (regenerative), the overall gain of the amplifier with feedback $\left(A_{f}\right)$ is given by,

$$
A_{f}=\frac{A}{1-A \beta}
$$

When $A \beta=1$, the denominator of the equation will be zero, and hence $A_{f}=$ Infinity. The gain becoming infinity means, there is output without any input. i.e. the amplifier becomes an oscillator. This condition $A \beta=1$, is known as Barkhausen criterion for oscillations.

Summarizing, the basic requirements for an oscillator are;

- A stable DC power supply source
- Anamplifier
- A regenerative (positive) feedback from outputto input
- A LC tank circuit to determine the frequency of oscillations

Starting signal for oscillators: As discussed above an oscillator gives alternating output voltage without an input signal once the amplifier is given a regenerative feedback. But in a practical oscillator circuit, to start off oscillations, no starting input signal is provided. However, the starting signal of an oscillator is generated by the noise voltage while switching on the oscillator circuit. Such noise voltages are produced due to the random motion of electrons in resistors used in the circuit.

Noise voltage contains almostall the sinusoidal frequencies of small amplitude. However, itgets amplified and appears at the outputterminals. The amplified noise now drives the feedback network, which is a resonant tank circuit. Because of this tuned tank circuit, the feedback voltage $A \beta$ is maximum at a particular frequency $f_{r}$, which will be the frequency of oscillations.

Further more, the phase shift required for positive feedback is correct at this frequency $f_{\text {r }}$ only. Thus although the noise voltage contains several frequency components, the output of the oscillator will contain a single sinusoidal frequency $f_{r}$ the resonant frequency of the tank circuit.

To summarize, the following are the requirements of an oscillator circuit to take-off with oscillations and have sustained oscillations,

- there must be positive feedback.
- Initially the loop gain product $A \beta$ must be $>1$.
- After the circuit starts oscillating, the loop gain product $A \beta$ must decrease to 1 and remain at 1 .
Hartley oscillator: One of the simplest of sinusoidal oscillators is the Hartley oscillator shown in Figs 9a and 9 b .

As in Fig 9a is a series fed Hartley oscillator. This circuit is similar to the tickler coil oscillator shown in Fig 7, but the tickler circuit coil $L_{\text {, }}$ is physically connected to $L$, and is hence a part of $L$ (like an auto-transformer). This oscillator is called series-fed because, the high frequency oscillations generated and the DC paths are the same, just as they would be in a series circuit. Series fed Hartley oscillators are not preferred due to their poor stability of oscillations.


Fig 9b is parallel fed Hartley oscillator commonly used in radio receivers. Parallel fed Hartley oscillators are known for their high stability of oscillations.

The circuit at Fig 9b is actually an amplifier with positive (regenerative) feedback to have sustained oscillations. The capacitor $\mathrm{C}_{2}$ and inductor $L_{2}$ form the path for RF current in the collector to ground circuit.

RF current through $L_{2}$ induces a voltage in $L_{1}$ in proper phase and amplitude to sustain oscillations.

The position of the tap at the junction of $L_{1}$ and $L_{2}$ determines how much signal is fed back to the base circuit.

The capacitor $C$ and the inductors $L_{1}+L_{2}$ forms the resonant tank circuit of the oscillator which determines the frequency of oscillations. Capacitor C can be made variable capacitor for tuning the oscillator to different frequencies. $C_{1}$ and $R_{1}$ form the $R C$ circuit which develops the bias voltage at the base.

The RF choke at the collector keeps the high frequency ac signal out of the $\mathrm{V}_{\mathrm{cc}}$ supply. In cheaper oscillator circuits the RF choke is omitted and is replaced by a resistor.

Resistor $R_{2}$ connected in the emitter provides DC stabilization. $R_{2}$ is by-passed by $C_{3}$ to prevent $A C$ degeneration.

The Hartley oscillator coil has three connections. These are usually coded on the coil. If they are not, it is generally possible to identify them by a resistance check. The resistance between the taps T and P as in Fig 10, is small compared with the resistance between $T$ and $G$., If the coil connections are not made properly, the oscillator will not work.

Fig 10


Checking oscillator frequency: The frequency of an oscillator can be computed if the values of $L\left(L=L_{1}+L_{2}\right)$ and C are known using the formula,

$$
f=\frac{1}{2 \pi \sqrt{L C}}
$$

where, $f$ is in hertz, $L$ in henry, and $C$ in farad.
The frequency of an oscillator may be measured in two ways,

- Using a direct read-out frequency meter also known as frequency counter which is most accurate, popular and easy to use.
- Using an oscilloscope with a calibrated time base to measure the period of the wave-form. From the measured period, ' $T$ ' frequency is calculated using the formula

$$
f=\frac{1}{T}
$$

where, $f$ is the frequency in Hz and ' $T$ ' the time period in seconds.

A practical Hartley oscillator circuit using medium-wave oscillator coil as L is shown in Fig 10.

The advantage of using a medium wave oscillator coil for $L$ is that the output can be taken out of the secondary winding (4 and 5 ) of the coil.

The transistor used is a silicon high frequency transistor (BF series) as the oscillator frequency is in the range of 1 MHz .

The divider biasing is provided to make the DC conditions such that the amplifier works as Class A. With the heavy feedback (large $\beta$ ), the large feedback signal drives the base of the transistor into saturation and cut-off. This large feedback signal produces negative DC clamping at the base, changing the operation from Class A to Class C. This negative clamping automatically adjusts the value of $A \beta$ to 1 . If the feedback is too large, it may result in loss of some of the output voltage because of the stray power loses.

When you build an oscillator, you can adjust the amount of feedback to maximize the output voltage. The trick is to use enough feedback to start under all conditions (different transistors, temperature, voltage etc.), but not so much that you lose more output than necessary.

The frequency of oscillations of the oscillator circuit at Fig 10 can be varied by varying the position of the shaft of the gang of the gang capacitor $\left(\mathrm{C}_{4}\right)$.

Colpitt's oscillator: Colpitt's oscillator is another type of sinusoidal oscillator or harmonic oscillator which uses a tank circuit for oscillations. Colpitt's oscillators are very popular and are widely used in commercial signal generators and communication receivers.

A typical Colpitt's oscillator is in Fig 11 is similar to a Hartley oscillator. The only difference is that the Colpitt's oscillator uses a split capacitor for the tank instead of a split inductor used in Hartley oscillators.

The parallel-fed or shunt-fed Colpitt's oscillator is in Fig 11, uses the common emitter configuration. The capacitors $C_{1 A} \& C_{1 B}$ from the voltage divider used to provide the feedback signal. The voltage drop across $\mathrm{C}_{1 \mathrm{~B}}$ determines the feedback voltage. All other components in this circuit have the same function as in the Hartley circuit.


The frequency of oscillations of the Colpitt's oscillator is given by,
$f=\frac{1}{2 \pi \sqrt{L C}}$
where,
f is the frequency of oscillation in hertz,
$L$ is the inductance of the coil in henry
C is the total capacitance in farad given by,
$C=\frac{C_{1 A} \times C_{1 B}}{C_{1 A}+C_{1 B}}$
The frequency of oscillations can be changed by using a miniature ganged capacitor for $\mathrm{C}_{1 \mathrm{~A}} \& \mathrm{C}_{1 \mathrm{~B}}$.

By varying the shaft of the ganged capacitor, both the capacitances $C_{1 A}$ and $C_{1 B}$ get varied, and hence, the frequency of oscillations of the oscillator varies.

Colpitt's oscillators are generally used for generating frequencies above 1 MHz .

A practical Colpitts oscillator circuit using a ganged capacitor for $\mathrm{C}_{1 \mathrm{~A}}$ and $\mathrm{C}_{1 \mathrm{~B}}$ and a medium wave oscillator coil for L is in Fig 12.


Crystal oscillators: The LC oscillator circuits such as Hartley and Colpitts have the problem of frequency instability. The most important reason for the frequency drift in LC oscillators is, the change in value of capacitance and inductance of the tank circuit that occurs when temperature changes.

As the temperature increases or decreases, the values of L and C deviate causing the circuit to oscillate at a frequency different from the desired resonant frequency. Other reasons for frequency deviation are, the leads of transistor, inter electrode and wiring capacitances.

The problem of frequency drift can be largely overcome by using high Q coils and good quality capacitors. But, with ordinary inductors and capacitors, $Q$-values in excess of a few hundred is very difficult or impossible to achieve.

Large improvements in frequency stability can be achieved by using a quartz crystal in the place of the conventional tuned circuit. Such oscillator circuits are referred to as crystal controlled oscillators.

Piezo-electric effect: It was discovered that certain crystals such as quartz and Rochelle salt, exhibit a special property known as piezo-electric property. A quartz crystal looks like a piece of thin frosted glass usually cut into $1 / 4$ to 1 inch squares as in Fig 13.


When such a crystal is held between two flat metal plates and pressed together, a small emf will be developed between the plates as if the crystal became a battery for an instant. When the plates are released, the crystal springs brings back to its original shape and an emf of opposite polarity is developed between the two plates. In this way, mechanical energy/force is converted to electrical energy by the crystal.

This property is made use of in the pick-ups for gramophone records. In a gramophone record, small mechanical vibrations are produced when the stylus tracks the groove on the gramophone plate. This vibrating force give rise to corresponding voltages representing the recorded sound at the pick-up terminals.

In addition to the above property of the crystal, when an emf is applied across the two plates of the crystal, the crystal will distort from its normal shape. If an opposite polarity emf is applied, the crystal will reverse its physical distorted shape. In this way, these crystals also convert electrical energy into mechanical energy.

The above two reciprocal actions of a crystal are known as piezo-electric effect. Such crystals are housed in crystal holders as in Fig 13.

Amongst several crystals having this piezo-electric property, the quartz crystal is most popular because, mechanical oscillations are started in this crystal it takes a long time for the oscillations to die away. Quartz crystals therefore, have a very high mechanical $Q$.

So far as the electrical properties are concerned, a quartz crystal is equivalent to the LC resonant circuit is in Fig 14.


The values of $L, R, C$ and $C_{m}$ depend upon the physical size of the crystal and how the crystal is cut from the original mass. Capacitance $C_{m}$ represents the mounting capacitance. For using the crystal in electronic circuits, two conducting electrodes are placed onto its two faces. Connecting leads are then joined to these electrodes. When the leads are connected to a source of oscillating voltage, mechanical vibrations are set up within the crystal.

If the frequency of the oscillating voltage is close to a resonant frequency of the crystal, then the crystal forces the oscillating voltage to coincide with the oscillating frequency of the crystal. Hence, in an oscillator, by using the crystal in the place of an LC resonant circuit, the frequency of oscillation is determined almost entirely by the crystal. Q values in excess of 20,000 are easily obtained with readily available crystals resulting in highly stable oscillating frequency.

Hence, when accuracy and stability of the oscillation frequency are important, a quartz crystal oscillator is used instead of Hartley or Colpitt's oscillators. The frequency range of crystals is usually between 0.5 to 30 MHz .

Pierce crystal oscillator: The pierce crystal controlled oscillator is in Fig 15 is often used because it requires very few components and has good frequency stability.

The pierce crystal oscillator is similar to the Colpitts oscillator but for the inductance coil replaced by a crystal. Here the crystal across the collector and the base terminals
of the transistor determines the oscillating frequency. As in a colpitts oscillator, capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ form a capacitive voltage divider for feedback. The ac voltage across $\mathrm{C}_{2}$ provides the necessary positive feedback to the base.

Fig 15


In Fig 15, the crystal acts like an inductor that resonates with $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$. In the base circuit, the $\mathrm{R}_{1} \mathrm{R}_{2}$ divider supplies forward bias voltage from the $\mathrm{V}_{\mathrm{CC}}$. Bias stabilization is provided by the $R_{E} C_{E}$ combination in the emitter circuit.

In Fig 15, if the crystal resonant frequency is, say 3579.545 Hz , then the oscillator oscillates at the same frequency and gives a sinusoidal output of 3579.545 Hz .

Crystal oscillators are generally used in,

- mobile radio transmitters and receivers
- broadcast transmitters
- test equipments such as signal generators where exact frequency and very high frequency stability are of utmost importance. The frequency drift in crystal controlled oscillators will be less than 1 Hz per $10^{6} \mathrm{~Hz}$.


## Multivibrator

It is a free running oscillator which gives repetitive pulse wave form output, and other types of multi-vibrators which are classified depending upon the manner in which the two stages of the multi-vibrator interchange their ON and OFF states. They are:

- Mono-stable multivibrator (having one stable state).
- Bistable multivibrator (having two stable states).


## Mono-stable Multivibrator

Fig 16 shows a typical mono-stable multi-vibrator also known as mono-shot or one-shot.

A mono-shot has one stable state with one transistor conducting and the other off. This state can be changed only temporarily by giving an input pulse generally known as trigger pulse to the transistor which is off. But this
changed state returns back to its original stable state after a period decided by the values of $R$ and $C$.


Fig 17 shows a practical mono-stable multi-vibrator with trigger input. Fig 17 also shows the wave-forms at different points of the circuit.


The period $t$ for which $Q_{2}$ is kept off temporarily is given by,

$$
\mathrm{t}=0.69 \mathrm{RC}
$$

Mono-stable multi-vibrators are extensively used as timers in electronic timing control circuits.

## Bistable multivibrator

An astable multi-vibrator automatically switches from one state to other (ON-to-OFF or OFF-to-ON...). Whereas, a bistable multi-vibrator will change the state(ON to OFF or OFF to ON) when triggered and remain in the new state (ON or OFF). This means, a bistable multi-vibrator has two stable states. Fig 18 shows a typical bistable multi-vibrator circuit.

The circuit at Fig 18 is completely symmetrical. The potential dividers $R_{1}, R_{2}$ and $R_{3}, R_{4}$ form identical bias network at the base of transistors. Each transistor is biased from the collector of the other transistor. Due to the slightest difference in parameters of the transistor, when the circuit is switched ON, any one of the two transistors will turn-ON, and the other remain in OFF condition.

In the circuit at Fig 18, the two identical CE amplifier stages are so connected that the output of one is fed to the input of the other, through resistors $\mathrm{R}_{1}, \mathrm{R}_{3}$ and shunted by capacitors $C_{1}, C_{2}$. The purpose of the capacitor is nothing but to speed up the switching characteristic of the circuit to get distortion-less output wave-form. Capacitors $\mathrm{C}_{1} \& \mathrm{C}_{2}$ are also known as commutating capacitors.


A bistable multi-vibrator is also known as a flip-flop. The output terminals are generally identified as $Q \& \bar{Q}$ (Q-bar) as in Fig 19.

When $Q$ is in high state (also known as Logic-1 state in digital electronics), $\overline{\mathrm{Q}}$ (Q-bar) will be in low state (also known as Logic-0 state), and vice versa. This circuit is known as a flip-flop circuit because, if one output flips(high/ logic-1) the other output automatically flops(low/logic-0). A flip-flop can be switched from one state to the other by applying a suitable triggering input. Flip-flops are used as a basic memory cell in digital computers for storing information. Flip-flops are used in various forms in almost all digital system as counters, frequency dividers and so on.


Practical bistable multi-vibrators with unsymmetrical and symmetrical triggering arrangement are shown in Fig 20a and 20b.


